REMARKS

In the Office Action, the Examiner noted that claims 1-23 are pending in the application, and that claims 1-23 are rejected. By this response, claim 15 is amended to correct a typographical error introduced by a previous amendment. Notably, a misspelling of the word "representation" has been corrected. In view of the following discussion, Applicants submit that none of the claims now pending in the application are non-enabled under the provisions of 35 U.S.C. §112 and anticipated under the provisions of 35 U.S.C. §102. Thus, Applicants believe that all of these claims are now in condition for allowance.

I. Rejection of Claims under 35 U.S.C. §112

The Examiner rejected claims 21-23 as being non-enabled by the specification. (Office Action, p. 2). The Examiner stated that while the specification describes associating an indicator across multiple levels of a hierarchy, the specification does not provide enablement for the hierarchical independence of the indicator. (Office Action, p. 2). Applicants respectfully disagree.

The term "hierarchically independent indication" is reasonably described in Applicants' specification such that one skilled in the art could make and use the invention without undue experimentation. Notably, Applicants' specification states: "As can be seen the connection name 'phase_x_0' assigned at the top level represents the phase connection of the clock driver at the top level to the down sampler in the bottom level and hence is [a] hierarchically independent indication." (Applicants' specification, paragraph 0036). Applicants' specification further states: "Note that the abstract connection is independent of the particular locations in the hierarchy of the clock driver or the down sampler, and is independent of the particular ways that connections may be made in VHDL." (Applicants' specification, paragraph 0037).

Thus, a hierarchically independent indicator is clearly described so as to be understood by one skilled in the art. A specific example of a hierarchically independent indicator is given (e.g., phase_x_0) in the context of an exemplary description of a downsampler. The relationship between the indicator phase_x_0 and other code portions of the downsampler is described and is attributed to the term "hierarchically independent indication."

As stated by the Federal circuit:

> A specification disclosure which contains a teaching of the manner and process or making and using the invention in terms which correspond in scope to those used in describing and defining the subject matter sought to be patented must be taken as in compliance with the enabling requirement of the first paragraph of §112 unless there is reason to doubt the objective truth of the statements contained therein.

Fiers v. Sugano, 25 USPQ2d 1601, 1607 (Fed. Cir. 1993). In addition, "[i]t has been consistently held that the first paragraph of 35 U.S.C. §112 required nothing more than objective enablement....How such a teaching is set forth, whether by the use of illustrative examples or by broad description terminology, is of no importance." Staehelin v. Secher, 24 USPQ2d 1513, 1516 (B.P.A.I. 1992) (citing In re Marzocchi, 169 USPQ 367 (C.C.P.A. 1971)). Applicants' specification describes the term "hierarchically independent indication" and relates such term to a specific example. In view of the foregoing, Applicants contend that claims 21-23 are enabled and fully satisfy the requirements of 35 U.S.C. §112. Accordingly, Applicants respectfully request the rejection of such claims be withdrawn.

II. Rejection of Claims Under 35 U.S.C. §102

The Examiner rejected claims 1-23 as being anticipated by Bening (United States patent 6,684,381, issued January 27, 2004). More specifically, in a previous response, Applicants argued that Bening does not teach translation of an electronic design representation into a circuit description language representation. In the present Office Action, the Examiner disagreed, stating that "Bening translates a hierarchical representation into a flat representation and, given a reasonably broad interpretation, an 'electronic design representation' is anticipated by the hierarchically representation...while 'a circuit description language representation' is anticipated by the flat representation." (Office Action, p. 4). The rejection is respectfully traversed.

Applicants have reviewed Bening and have not found any disclosure of translating a hierarchical representation into a flat representation. The only translation performed by Bening is the translation of regular expressions embedded in HDL code into explicit repetitive HDL code. As stated in Bening, the method 100 of FIG. 1 elaborates HDL code that uses regular expressions to represent hardware description

into code that provides an explicit detailed description of the hardware. (Bening, col. 6, lines 1-8). Thus, Bening starts with HDL code, processes the HDL code, and ends with HDL code.

In Applicants' invention, an electronic design representation is translated into a circuit description language representation. The Examiner argues that the terms "electronic design representation" and "circuit description language representation" are equivalent in that the HDL-to-HDL translation performed by Bening anticipates Applicants' claim 1. The terms, however, cannot be interpreted separately in a vacuum. Rather, the claim must be read in its entirety and in light of the specification. The term "electronic design representation" cannot be read by itself, but rather in conjunction with the term "circuit description language representation" and Applicants' specification.

The terms "electronic design representation" and "circuit description language representation" are two different representations as evidenced by their different names and as set forth in Applicants' specification. The circuit description language representation may include an HDL representation (i.e., a circuit description language). In contrast, the electronic design representation does not encompass an HDL representation. (See Applicants' specification, paragraphs 0022 and 0023). This is also evidenced by claim 1, as there is no "circuit description language" modifier in the term "electronic design representation."

If the HDL code resulting from the method 100 in Bening is used to read on the circuit description language representation of Applicants' invention, then Bening must teach some representation other than HDL to read on the electronic design representation. Bening, however, does not teach this other non-HDL representation. Rather, the input to the method 100 of Bening is an HDL representation. Therefore, Bening does not teach each and every element of Applicants' claim 1.

Note that Applicants are not attempting to read limitations from the specification into the claims. Rather, the specification provides evidence that the use of two different terms in claim 1 (electronic design representation versus circuit description language representation) equate to two different representations. Thus, when claim 1 is read in light of the specification, it is clear that the electronic design representation is different than a circuit description language representation. A single circuit description

language representation, i.e., HDL code, cannot anticipate two different representations. The same holds true for a hierarchical representation and a flat representation of HDL code. Since the term "electronic design representation" does not encompass an HDL representation, as evidenced by the use of two different terms in claim 1 and by the specification, a hierarchical HDL representation or any other HDL representation does not teach or suggest an electronic design representation, as recited in Applicants' claim 1.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984). Since Bening does not teach translating an electronic design representation into a circuit description language representation, Bening does not teach each and every element of Applicants' claim 1 as arranged therein.

Independent claims 6, 11, 13, 15, and 18, each recite, among other features, translation or production of a circuit description language representation from an electronic design representation of an integrated circuit. For the reasons discussed above, Applicants contend that Bening also fails to anticipate claims 6, 11, 13, 15, and 18. Independent claim 21 recites steps of identifying a plurality of ports that require connection, associating with a first port a hierarchically independent indication that a first port is connected to a second port, and connecting the first port to the second port in a circuit description language representation using the hierarchically independent indication. Bening does not teach or suggest such features. In particular, Bening does not teach or suggest connection of ports in a circuit description language representation using a hierarchically independent indication. Thus, Bening also fails to anticipate claim 21.

Claims 2-5, 7-10, 12, 14, 16-17, 19-20, and 22-23 depend, either directly or indirectly, from claims 1, 6, 11, 13, 15, 18, and 21 and recite additional features therefor. Since Bening does not anticipate Applicants' invention as recited in claims 1, 6, 11, 13, 15, 18, and 21, dependent claims 2-5, 7-10, 12, 14, 16-17, 19-20, and 22-23 are also not anticipated and are allowable.

In view of the foregoing, Applicants contend that claims 1-23 are not anticipated by Bening and, as such, fully satisfy the requirements of 35 U.S.C. §102. As such, Applicants respectfully request that the rejection of such claims be withdrawn.

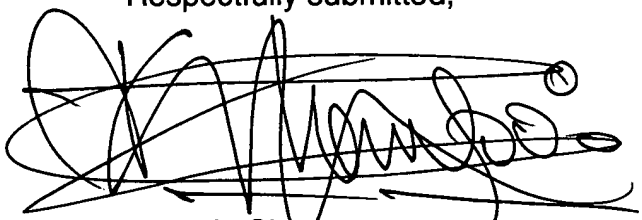
CONCLUSION

Thus, Applicants submit that none of the claims presently in the application are non-enabled under the provisions of 35 U.S.C. §112 or anticipated under the provisions of 35 U.S.C. §102. Consequently, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Keith A. Chanroo at (408) 879-7710 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on November 7, 2006.

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